USB FIFO - Fast Parallel Data Transfer IC

FEATURES

- Single Chip Fast Data Transfer Solution
- Send / Receive Data over USB at up to 1 M Bytes / sec
- 384 byte FIFO Transmit buffer / 128 byte FIFO receive buffer for high data throughput
- Simple interface to CPU or MCU bus
- No in-depth knowledge of USB required as all USB Protocol is handled automatically within the I.C.
- FTDI's Virtual COM port drivers eliminate the need for USB driver development in most cases.
- Compact 32 pin (7mm x 7mm) MQFP package
- Integrated 6MHz - 48MHz Clock Multiplier aids FCC and CE compliance
- Integrated 3.3v Regulator – No External Regulator Required
- 4.4v .. 5.25v Single Supply Operation
- UHCI / OHCI Compliant
- USB 1.1 Specification Compliant
- USB VID, PID, Serial Number and Product Description Strings in external E2PROM.

Virtual COM Port Drivers for –

Windows 98 and Windows 98 SE
Windows 2000
Windows Millennium **
Apple iMAC **
Linux **

- Application Areas

USB ISDN and ADSL Modems
High Speed USB ⇔ PDA Communications
USB I/F for Digital Cameras
USB I/F for MP3 players
High Speed USB Instrumentation
USB ⇔ USB data transfer cables
USB ⇔ USB null-modem cables

GENERAL DESCRIPTION

The FT8U245AM provides an easy cost-effective method of transferring data to / from a peripheral and a host P.C. at up to 8 Million bits (1 Megabyte) per second. It's simple FIFO-like design makes it easy to interface to any CPU (MCU) either by mapping the device into the Memory / IO map of the CPU, using DMA or controlling the device via IO ports.

To send data from the peripheral to the host P.C. simply write the byte wide data into the device when the transmitter empty status bit is not active. If the (384 byte) transmit buffer fills up, the device de-asserts transmit empty in order to stop further data being written to the device until some of the FIFO data has been transferred over USB.

When the host P.C. sends data to the peripheral over USB, the device will assert the receiver full status bit to let the peripheral know that data is available. The peripheral then reads the data until the receiver full status bit goes inactive, indicating no more data is available to read.

By using FTDI's virtual COM Port drivers, the peripheral looks like a standard COM Port to the application software. Commands to set the baud rate are ignored – the device always transfers data at it's fastest rate regardless of the application's baud rate setting.

FT8U245AM - FUNCTIONAL BLOCK DESCRIPTION

- **3.3V LDO Regulator**

  The 3.3V LDO Regulator generates the 3.3 volt reference voltage for driving the USB transceiver cell output buffers. It requires an external decoupling capacitor to be attached to the 3V3OUT regulator output pin.

- **USB Transceiver**

  The USB Transceiver Cell provides the USB 1.1 full-speed physical interface to the USB cable. The output drivers provide 3.3 volt level slew rate control signalling, whilst a differential receiver and two single ended receivers provide USB data in, SEO and USB Reset condition detection.

- **USB DPLL**

  The USB DPLL cell locks on to the incoming NRZI USB data and provides separate recovered clock and data signals to the SIE block.

- **6MHz Oscillator**

  The 6MHz Oscillator cell generates a 6MHz reference clock input to the X8 Clock multiplier from an external 6MHz crystal or ceramic resonator.

- **X8 Clock Multiplier**

  The X8 Clock Multiplier takes the 6MHz input from the Oscillator cell and generates a 12MHz reference clock for the SIE, USB Protocol Engine and UART FIFO controller blocks. It also generates a 48MHz reference clock for the USB DPPL and the Baud Rate Generator blocks.

- **Serial Interface Engine (SIE)**

  The Serial Interface Engine (SIE) block performs the Parallel to Serial and Serial to Parallel conversion of the USB data. In accordance to the USB 1.1 specification, it performs bit stuffing / un-stuffing and CRC5 / CRC16 generation / checking on the USB data stream.

- **USB Protocol Engine**

  The USB Protocol Engine manages the data stream from the device USB control endpoint. It handles the low level USB protocol (Chapter 9) requests generated by the USB host controller and the commands for controlling the functional parameters of the UART.

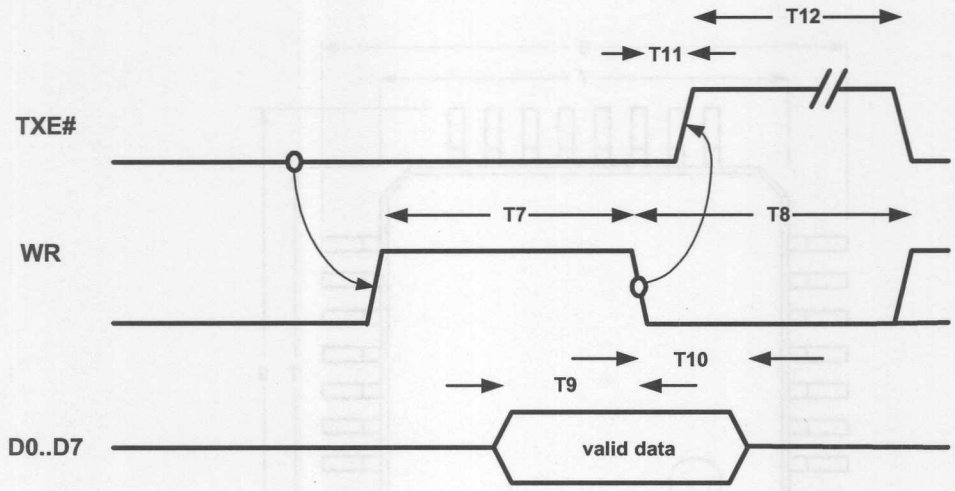
- **Fifo Receive Buffer (128 bytes)**

  Data sent from the USB Host to the FIFO via the USB data out endpoint is stored in the FIFO Receive Buffer and is removed from the buffer by reading the FIFO contents using RD#.

Table 1 - FT8U245AM - PINOUT DESCRIPTION

Pin #	Signal	Type	Description
7	USBDP	I/O	USB Data Signal Plus – Requires 1.5k pull-up to 3V3OUT
8	USBDM	I/O	USB Data Signal Minus
6	3V3OUT	OUT	3.3 volt Output from integrated regulator
27	XTIN	IN	Input to 6MHz Crystal Oscillator Cell
28	XTOUT	OUT	Output from 6MHz Crystal Oscillator Cell
31	RCCLK	I/O	RC timer – used to guarantee clock stability on exiting sleep mode. Clamped low during reset or sleep condition.
4	RESET#	IN	Resets entire device using external RC network
32	EECS	I/O	Optional EEPROM – Chip Select
1	EESK	I/O	Optional EEPROM – Clock
2	EEDATA	I/O	Optional EEPROM – Data I/O
5	TEST	IN	Puts device in i.c. test mode – must be tied to GND
25	D0	I/O	Bi-directional Data Bus Bit # 0
24	D1	I/O	Bi-directional Data Bus Bit # 1
23	D2	I/O	Bi-directional Data Bus Bit # 2
22	D3	I/O	Bi-directional Data Bus Bit # 3
21	D4	I/O	Bi-directional Data Bus Bit # 4
20	D5	I/O	Bi-directional Data Bus Bit # 5
19	D6	I/O	Bi-directional Data Bus Bit # 6
18	D7	I/O	Bi-directional Data Bus Bit # 7
16	RD#	IN	Enables Current FIFO Data Byte on D0..D7.when low. Fetches the next FIFO Data Byte (if available) from the Receive FIFO Buffer when RD# goes from low to high.
15	WR	IN	Writes the Data Byte on the D0..D7 into the Transmit FIFO Buffer when WR goes from high to low.
14	TXE#	OUT	When high, do not write data into the FIFO. When low, data can be written into the FIFO by strobing WR high then low.
12	RXF#	OUT	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by strobing RD# low then high again.
11	EEREQ#	IN	Requests the EEPROM contents to be accessed via the Data Bus.
10	EEGNT#	OUT	When low, allows the EEPROM contents to be accessed via the Data Bus.
3,13,26	VCC	PWR	Device - +4.4 volt to +5.25 volt Power Supply Pins
9.17	GND	PWR	Device – Ground Supply Pins
30	AVCC	PWR	Device - Analog Power Supply for the internal x8 clock multiplier
29	AGND	PWR	Device - Analog Ground Supply for the internal x8 clock multiplier

FT8U245AM TIMING DIAGRAM – FIFO WRITE CYCLE



Time	Description	Min	Max	Unit
T7	WR Active Pulse Width	50		ns
T8	WR to WR Pre-Charge Time	50		ns
T9	Data Setup Time before WR inactive		20	ns
T10	Data Hold Time from WR inactive	10		ns
T11	WR Inactive to TXE#	5	25	ns
T12	TXE inactive after RD cycle	80		ns

Absolute Maximum Ratings

Storage Temperature	-65°C to + 150°C
Ambient Temperature (Power Applied)	0°C to + 70°C
VCC Supply Voltage	-0.5v to +6.00v
DC Input Voltage - Inputs	-0.5v to VCC + 0.5v
DC Input Voltage - High Impedance Bidirectionals	-0.5v to VCC + 0.5v
DC Output Current – Outputs	24mA
DC Output Current – Low Impedance Bidirectionals	24mA
Power Dissipation	500mW

DC Characteristics (Ambient Temperature = 0 .. 70 Degrees C)

	Description	*Min*	*Max*	*Units*	*Conditions*
VCC	Operating Supply Voltage	4.4	5.25	v	
Icc1	Operating Supply Current		50	mA	Normal Operation
Icc2	Operating Supply Current		250	uA	USB Suspend
Ioh1	Digital IO Pins Source Current	4		mA	Voh = VCC – 0.5v
Iol1	Digital IO Pins Sink Current	4		mA	Vol = + 0.5v
Voh1	Input Voltage Threshold (Low)		0.6	v	
Vol1	Input Voltage Threshold (High)	2.7		v	
VDif	USB Differential Input Sensitivity	0.2		v	
VCom	USB Differential Common Mode	0.8	2.5	v	
URxt	USB Single Ended Rx Threshold	0.8	2.0	v	
UVh	USB IO Pins Static Output (Low)		0.3v		Rl = 1.5k to 3.6v
UVl	USB IO Pins Static Output (High)	2.8			Rl = 15k to GND